SPYROS TRAGOUDAS

1. SCHOLARLY ACTIVITIES

Research interests: Embedded systems, VLSI design and test automation, and machine learning.

Summary of accomplishments and distinctions:

- 2023 Inventor of the Year award at the SIU System which includes three campuses (SIUC, the SIU School of Medicine, and SIU Edwardsville).
- 2005 Outstanding SIUC Research Faculty Award.
- 2004 Outstanding Research Faculty Award in the College of Engineering at SIUC.
- Awarded approximately $8.5M in extramural funding (about $7.9M as the principal investigator and fiscal officer, and about $600K as a co-PI), and several equipment donations.
- Research publications: About 100 peer-reviewed journals, over 200 papers in conference proceedings (including five best paper awards), and 7 book chapters.
- Delivered 6 keynote speeches and distinguished lectures.
- Holds 6 US patents.
- Supervised 34 doctoral dissertations, 84 MS theses, and supported 19 undergraduate students with NSF awards.
- Served or serves on the Editorial Board of several journals, such as the IEEE Transactions on Computers, and conference program committees, such as the IEEE International Conference of Computer-Aided Design.
- Co-founded and directed two NSF Industry-University Cooperative Research Centers (IUCRCs) at SIUC.

Director of externally funded research centers (4/1/2009 to date)

1. **Intelligent, Distributed, Embedded Applications and Systems (IDEAS), an NSF Industry-University Cooperative Research Center (IUCRC), 2023 - 2028**: IDEAS is a three-university center between Arizona State University (ASU), Southern Illinois University Carbondale, and the University of Southern California. that is funded by the National Foundation (NSF). Directs the SIUC site, recruits member companies, and is the PI or co-PI in research grants through the center.
2. **Consortium for Embedded Systems at SIUC, since 2022 (approved by the Illinois Board of Higher Education):** The center is exclusively funded by the membership fees of member companies he has recruited.
3. **Center for Embedded Systems (CES), an NSF Industry-University Cooperative Research Center (IUCRC), 2009-2022:** The participating university sites were ASU and SIUC. Served as the center's site director at SIUC. Recruited fifteen companies at the SIUC site. Was the PI of center projects that totaled about $2.8M.

Recent extramural research awards

1. In-Field Circuit Monitoring with Machine Learning, Agency: National Science Foundation - IDEAS IUCRC through ASU subaward ASU/NSF-ASUB00001597. PI: S. Tragoudas. Duration: 11/1/23-2/28/28.
2. DNN Architectural Enhancements with Inference Time and Energy Considerations. Agency: National Science Foundation - IDEAS IUCRC through an ASU subaward. PI: S. Tragoudas. Duration: 11/1/24-2/28/28.
3. Improving the Accuracy of Ultrasound-based Canopy Volume Estimation via Correlation Detection Methods. Agency: National Science Foundation - IDEAS IUCRC through an ASU subaward. PI: H. Wang. Co-PIs: J. Qin and S. Tragoudas. Duration: 11/1/24-2/28/28.
4. AI-Assisted Characterization and Reduction of Point Cloud Noise. Agency: National Science Foundation - IDEAS IUCRC through ASU subaward ASU/NSF-ASUB00001598. PI: S. Tragoudas. Co-PI: H. Wang. Duration: 11/1/23-2/28/28.
5. DESC: Type I: Towards Greener AI Computing: Designing and Managing Sustainable Heterogeneous Data Centers. Agency: National Science Foundation (CCF 2324854). PI: I. Anagnostopoulos, co-PI: S. Tragoudas. Duration: 9/1/2023 – 8/31/2026.
6. Intelligent, Distributed, Embedded Applications and Systems (IDEAS), an NSF Industry-University Cooperative Research Center, Agency: National Science Foundation. PI: S. Tragoudas, co-PI: H. Wang. Duration: 3/15/23 – 2/29/28. $610,000 main award (CNS 2231623), $110,000 supplemental funding (EFMA 2405058), and $16,000 REU supplement.

7. Consortium for Embedded Systems at SIU. Awards from AMD, Ameren, and Collins Aerospace. PI: S. Tragoudas. Duration: 7/1/22 – 6/30/23.
8. NSF IUCRC Consortium for Embedded Systems – SIUC site. Awards from AMD, Collins Ameren, Ford. PI: S. Tragoudas. Duration: 4/16/21 – 3/31/22.
9. Modular and Scalable Sustainable Infrastructure for the SIUC campus. Agency: US Department of Energy & the Illinois Environmental Protection Agency. PI: S. Tragoudas, co-PIs: C. Hatziadoniu, H. Wang, I. Anagnostopoulos, G. Baduge, and A. Komaee. Duration: 9/19 – 6/21.
10. NSF IUCRC Consortium for Embedded Systems – SIUC site. Awards from AMD, Ameren, Collins Aerospace, Intel, Ford. PI: S. Tragoudas. Duration: 4/16/20 - 4/15/21.
11. NSF IUCRC Consortium for Embedded Systems – SIUC site. Awards from AMD, Collins Aerospace, Intel, Los Alamos National Lab, Ford, and General Motors ($50,000). PI: S. Tragoudas. Duration: 4/16/19 - 4/15/20.
12. Planning IUCRC: Southern Illinois University Carbondale - Center for Networked, Embedded, Smart, and Trusted Things (NESTT). Agency: National Science Foundation (IIP 1822155). PI: S. Tragoudas. Duration: 08/03/2018- 07/02/2019
13. Collaborative Research: Consortium for Embedded Systems – Phase II. Agency: National Science Foundation (IIP 1361847). PI: S. Tragoudas. Duration: 04/07/2014-03/31/2022.
14. Collaborative Research: Consortium for Embedded Systems – Phase II (REU). Agency: National Science Foundation (IIP 1447290). PI: S. Tragoudas. Duration: 01/28/2015-03/31/2021.
15. NSF IUCRC Consortium for Embedded Systems – SIUC site. Awards from Intel, Ford, and United Technologies. PI: S. Tragoudas. Duration: 4/16/18 - 4/15/19.
16. Investigation of acoustic-based energy harvesting and data communication for sensors enclosed in metal valves. Amount: Award from Emerson. PI: S. Tragoudas, Co-PI: H. Wang. Duration: 1/1/18-12/31/2021.

Recent peer-reviewed journal publications

Ph.D. or MS students supervised at the time of publication denoted in italics

1. *H.B.M. Senarathna,* S. Tragoudas. J. Wibbenmeyer and N. Khdeer, Time Series Analysis Neural Networks for Detecting False Data Injection Attacks of Different Rates on Power Grid State Estimation, ACM Transactions on Privacy and Security, to appear in 2025.
2. *V. Pentsos,* S. Tragoudas. J. Wibbenmeyer and N. Khdeer, A Hybrid LSTM-Transformer Model for Power Load Forecasting, IEEE Transactions on Smart Grid, to appear in 2025.. Early access https://ieeexplore.ieee.org/document/10887006
3. *B.R. Paudel* and S. Tragoudas. Memristive Crossbar Arrays-based Adversarial Defense using Compression, IEEE Transactions of Emerging Technologies in Computing (TETC), vol. 12, issue 3, pp. 864-877, July 2024. https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=10271126
4. *X. Chen,* L. Gupta, and *S.* Tragoudas, Improving the Forecasting and Classification of Extreme Events in Imbalanced Time Series Through Block Resampling in the Joint Predictor-Forecast Space, IEEE Access, vol. 10, pp. 121048-121079, vol. 10, 2022, (11/4/2022), DOI: 10.1109/ACCESS.2022.3219832
5. *K. Gnawali,* S. Tragoudas. High-Speed Memristive Ternary Content Addressable Memory, IEEE Transactions on Emerging Topics in Computing (TETC), vol. 10, issue 3, pp. 1349-1360, 2021.
6. *K. Gnawali,* S. Tragoudas, and H. Quinn. Developing Benchmarks for Radiation Testing of Microcontroller Arithmetic Units using ATPG, IEEE Transactions on Nuclear Science, vol. 68, no. 5. pp.857-864, May 2021.
7. *K. Gnawali,* H. Quinn, and S. Tragoudas. Updates on Testing Microprocessors Effectively, IEEE Transactions on Nuclear Science (TNS), vol. 68, no. 5, pp.842-849, May 2021.
8. *A. Watkins* and S. Tragoudas. Radiation Hardened Latch Designs for Double and Triple Node Upsets, IEEE Trans. on Emerging Topics in Computing (TETC), vol. 8, no. 3, pp. 616-626, July-September 2020.
9. *P.K. Javvaji* and S. Tragoudas. Test pattern Generation and Critical Path Selection in the Presence of Statistical Delays, IEEE Trans. on Very Large-Scale Integration Systems (TVLSI), pp. 163-173, vol. 28, no.1, January 2020.
10. *K. P. Gnawali, B.R. Paudel,* and S. Tragoudas. Reliability Enhancements in Memristive Neural Network Architectures, IEEE Transactions on Nanotechnology (TNANO), vol. 18, pp.866-878, August 2019.
11. *P.K. Javvaji* and S. Tragoudas. On the Sensitization Probability of a Critical Path Considering Process Variations and Path Correlations, IEEE Transactions on Very Large-Scale Integration Systems (TVLSI), pp. 1196-1205, vol. 27, issue.5. May 2019.
12. *K. P. Gnawali, S. N. Mozaffari,* and S. Tragoudas. Low Power Spintronic Ternary Content Addressable Memory, IEEE Transactions on Nanotechnology (TNANO), pp. 1206-1216, vol. 17, no. 6, Nov. 2018.

13. *K. P. Gnawali, S. N. Mozaffari,* and S. Tragoudas. Low Power Artificial Neural Network Architectures, IEEE VLSI Circuits and Systems Letter, pp. 0-5, vol.4. issue 4, Nov. 2018, https://arxiv.org/pdf/1904.02183.pdf
14. *S. N. Mozaffari* and S. Tragoudas. Maximizing the number of threshold logic functions using resistive memory, IEEE Transactions on Nanotechnology (TNANO), pp. 897-905, vol. 12, no. 5. September 2018.
15. *S. N. Mozaffari*, S. Tragoudas, and Th. Haniotakis. A generalized approach to implement efficient CMOS-based threshold logic functions, IEEE Trans. on Circuits and Systems I (TCAS-I), pp. 946-.959, vol.65, no.3. Mar. 2018
16. S. Leitner, H. Wang, and S. Tragoudas. Design of Scalable Hardware-Efficient Compressive Sensing Image Sensors, IEEE Sensors Journal, pp.641-651, vol. 18, no.2. January 2018.

Recent publications in peer-reviewed conference proceedings

Ph.D. or MS students supervised denoted in italics

1. *V. Pentsos,* S. Tragoudas,,K.N. Gowda, and M. Schmit. Energy-Aware DNN Task Scheduling with Dynamic Batching and Frequency Adjustment, Proc. of the 26th IEEE International Symposium on Quality of Electronic Design (ISQED), San Francisco, CA, April 22-25, 2025
2. *D.M. Lama Hewage, D. Senarathna,* and S. Tragoudas. Enhanced Distribution Matching for Multiclass Quantification. IEEE Intl Conf. on Machine Learning and Applications (ICMLA), December 2024, Miami, FL.
3. *B.R. Paudel,* H. Wang, and S. Tragoudas. High Precision Winner-Take-All Circuit for Neural Networks. Proc. of the 36th IEEE International System-on-Chip Conference (SOCC), September 5-8, 2023, Santa Clara, CA.
4. *D. Senarathna* and S. Tragoudas. Deep Neural Network Accelerators for Repetitive Boolean Function Evaluation. Proc. 36th IEEE International System-on-Chip Conference (SOCC), September 5-8, 2023, Santa Clara, CA.
5. *D. Senarathna, R. Ferdous,* and S. Tragoudas. An Enhanced YOLO Failure Detection Method. Proc. of the 22nd IEEE Int'l Conf. on Machine Learning and Applications (ICMLA), December 15-17, 2023, Jacksonville, FL.
6. *D. Senarathna,* S. Tragoudas, K.N. Gowda, and M. Schmit, Detection and Quantization of Data Drift in Image Classification Neural Networks, International Workshop on Resource-Constraint Machine Learning (RCML) 2023, Proc. of the 24th IEEE Intl Conference on High-Performance Switching and Routing (HPSR), June 5-7, 2023.
7. *D. Senarathna,* S. Tragoudas, J. Wibbenmeyer, and N. Khdeer, Increasing Detection Rate of False Data Injection Attacks Using Measurement Predictors, Proc. IEEE Intl Conf. on Smart Energy Grid Engineering (SEGE), 13-15 Aug. 2023.
8. *V. Pentsos* and S. Tragoudas, A statistical approach to improve CNN classification accuracy, International Workshop on Resource-Constraint Machine Learning (RCML) 2023, in the Proceedings of 24th IEEE International Conference on High-Performance Switching and Routing (HPSR), June 5-7, 2023.
9. *V. Pentsos,* S. Tragoudas, J. Wibbenmeyer, and N. Khdeer, Optimizing Multivariate LSTM on real-world data for power load forecasting, Proc. 11th IEEE Intl Conf. on Smart Energy Grid Engineering (SEGE), 13-15 Aug. 2023.
10. *B.R. Paudel* and S. Tragoudas*,* Adversarial Defense Using Memristors and Input Preprocessing, 2023 IEEE International Symposium on Circuits and Systems (ISCAS), Monterey, California, May 21-23, 2023.
11. *B.R. Paudel* and S. Tragoudas*,* The Impact of on-chip Training to Adversarial Attacks in Memristive Crossbar Arrays, International Test Conference (ITC), September 25-30, 2022, Anaheim CA.
12. *B.R. Paudel and S. Tragoudas,* Compressed Learning in MCA Architectures to Tolerate Malicious Noise, IEEE Int' Symp. on On-Line Testing and Robust Systems Design (IOLTS), September 12-14, 2022, Torino IT
13. *B.R. Paudel, V.Pentsos,* and S. Tragoudas, On the Resiliency of an Analog Memristive Architecture against Adversarial Attacks, Proc. IEEE Intl Symp. on the Quality of Electronic Design (ISQED), March 2022. *(Invited)*
14. *H. Senarathna* and S. Tragoudas. Computation of Soft Error Rates considering Test Pattern Sequences, Proc. of the 2022 IEEE Intern. Symp. on Quality of Electronic Design (ISQED), Santa Clara, CA, March 2022.
15. *B.R. Paudel, H.B.M. Senarathna,* H. Wang*,* S.Tragoudas*,* Y. Hu, and S. Jiang, Predicting YOLO Misdetection by Learning Grid Cell Consensus, Proceedings of the 20th IEEE International Conference on Machine Learning and Applications (ICMLA), December 13-16, 2021, Pasadena, CA.
16. *V. Pentsos, B.R. Paudel,* S.Tragoudas, K.N. Gowda, and M. Schmit, Improved CNN Classification Accuracy with the Addition of Shallow Cascading CNNs, Proceedings of the 20th IEEE International Conference on Machine Learning and Applications (ICMLA), December 13-16, 2021, Pasadena, CA.
17. *B.R. Paudel, A. Itani,* and S.Tragoudas, Adversarial Robustness Assessment and Defense in SNN against Black Box Attacks, Proceedings of the 20th IEEE International Conference on Machine Learning and Applications (ICMLA), December 13-16, 2021, Pasadena, CA.

18. *P. Savanur* and S.Tragoudas*,* A Fault Model to Detect Design Errors in Combinational Circuits, Proceedings of the 34th IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), October 6-8, 2021, Athens, Greece (virtual).
19. *B. Shanyour,* and S. Tragoudas, Broadside ATPG for Low Power Trojans Detection using Built-in Current Sensors, Proceedings of the 26th IEE International Symposium on On-Line, Testing and Robust System Design, July 13-15, 2020, Naples, Italy.
20. *K. Gnawali,* S. Tragoudas, and H. Quinn. Updates on Testing Microprocessors Effectively, Proceedings of the 2020 Nuclear and Space Radiation Effects Conference (NSREC), July 20-24, 2020, Santa Fe, NM.
21. *K. Gnawali,* H. Quinn, and S. Tragoudas. Developing Benchmarks for Radiation Testing of Microcontroller Arithmetic Units using ATPG, Proc. Nuclear and Space Radiation Effects Conf. (NSREC), July 20-24, 2020, Santa Fe, NM.
22. *B. Shanyour,* S. Tragoudas, Detection of Low Power Trojans in Standard Cell Designs using Built-In Current Sensors, Proc. 2018 International Test Conference (ITC), October 28- November 2, 2018, Phoenix, AZ.
23. *S.N. Mozaffari, K.P. Gnawali,* and S. Tragoudas, An aging resilient neural network architecture, Proceedings of the IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH), July 2018, Athens, Greece.
24. *P. Javvaji,* S. Tragoudas, A method to model statistical path delays for accurate defect coverage, Proceedings of the 31st IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), October 8-10, 2018, Chicago, IL
25. *P. Savanur,* S. Tragoudas, Threshold Voltage Extraction using NBTI aging, Proceedings of the 31st IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), October 8-10, 2018, Chicago, IL
26. *P. Javvaji,* S. Tragoudas, and G. Kondapuram*,* Scalable fault coverage estimation in sequential circuits without fault injection, Proceedings of the 2018 IEEE International Symposium on Circuits and Systems (ISCAS), May 27-30, 2018, Florence, Italy.
27. *P. Javajji*, *B. Sanyour* and S. Tragoudas, Test set identification for improved delay coverage in the presence of statistical delays, Proceedings of the 2018 IEEE International Symposium on Quality of Electronic Design (ISQED), March 13-14, 2018, Santa Clara, CA.

Supervised Ph.D. Dissertations

1. Herath Senarathna Danushka, Trustworthy Embedded Systems based on Deep Neural Networks, School of Electrical Computer and Biomedical Eng., SIUC, January 2025. Currently with Synopsys Inc., Sunnyvale, CA
2. Xiaoqian Chen, Imbalanced Time Series Forecasting and Neural Time-series Classification, School of Electrical Computer and Biomedical Eng., SIUC, August 2023. Currently a Postdoc at Emory University School of Medicine, Atlanta, GA.
3. Bijay Raj Paudel, Accuracy Considerations in Deep Learning using Memristive Crossbar Arrays, School of Electrical Computer and Biomedical Eng., SIUC, December 2022. Currently with Intel Corp., Santa Clara CA.
4. Ramesh Puneet Savanur. Techniques to Address Manufacturing Defects in Deep Sub-micron, School of Electrical Computer and Biomedical Eng., SIUC, April 2022. Currently with Nvidia Corp., Santa Clara CA.
5. Krishna Gnawali, Emerging Memory-based Designs and Resiliency to Radiation Effects, School of Electrical Computer and Biomedical Eng., SIUC, October 2020. Currently with Synopsys Corp., Mountain View, CA.
6. Basim Shanyour, Testing and Security considerations in the presence of process variations, ECE Dept.., SIUC, March 2020. Currently with Qualcomm Corporation, San Diego, CA
7. Pavan Kumar Javvaji, Statistical Methods for Critical Path Selection and Fault Coverage in Integrated Circuits, ECE Dept.., SIUC, May 2019. Currently with Nvidia Corporation, Santa Clara, CA.
8. Wisam Al-Jubouri, Measuring the Delay of Embedded Segments in Integrated Circuits using Current Sensors, ECE Dept.., SIUC, October 25, 2018. Currently with Microchip Technology Inc., Phoenix AZ, Previously with Cadence Inc., NY.
9. Seyed Nima Mozaffari, Design and Test of Digital Circuits and Systems Using CMOS and Emerging Resistive Devices, ECE Dept., SIUC, March 2018. Currently with Nvidia Corp., Santa Clara, CA.
10. Adam Watkins, Analysis and Mitigation of Multiple Radiation Induced Errors in Modern Circuits, ECE Dept., SIUC, November 2016. Currently with Amazon, Space and Radiation, Seattle, WA. Previously with Los Alamos National Labs.
11. Joseph Lenox, Parallel and Fault Grading Heuristic and Testing Approaches to Trojan IC Detection, ECE Dept., SIUC, October 2016. Currently with Collins Aerospace, Cedar Rapids, IA.

12. Luke Pierce, Testing and Security Related Considerations in Embedded Software, ECE Dept., SIUC, August 2016. Currently with Amazon Web Services, Portland, OR.
13. Phaninder Alladi, Validation of Circuit Timing Behavior in the Presence of Delay Defects and NBTI aging, ECE Dept., SIUC, August 2016. Currently with Qualcomm Corporation, San Diego, CA. Previosuly with Synopsys Inc., Mountain View, CA.
14. Ahish Mysore Somashekar, Methodologies for Test and Diagnosis of Delay Defects in Integrated Circuits, ECE Dept., SIUC, December 2015. Currently with Intel Corporation, Santa Clara, CA.
15. Pragyan (Sheela) Mohanty, Function-based Algorithms for Biological Sequences, ECE Dept., SIUC, December 2015. Currently with Sierra Nevada Corporation, Reno, NV.
16. Chandra Babu Dara, Design High-Performance Threshold Logic Gates, ECE Dept., SIUC, December 2015. Currently with Broadcom Corporation, San Jose, CA.
17. Ashok Kumar Palaniswamy, Synthesis and Testing of Threshold Logic Circuits, ECE Dept., SIUC, July 2014. Currently DFT engineer with Qualcomm. Previously with Synopsys Corporation, Mountain View, CA.
18. Kedar Karmakar, Scalable bus encoding for error-resilient high-speed on-chip communication, ECE Dept., SIUC, June 2013. Currently with Intel Corporation, Hillsboro, OR.
19. Sreenivas Gangadhar, Analytical Methods to Propagate and Diagnose Single Event Transients, ECE Dept., SIUC, August 2012. Currently DFT Director at Microsoft, Austin TX. Previously, Intel Corporation, Austin, TX.
20. Dheepakkumaran Jayaraman, Optimization Techniques for Performance and Power Dissipation in Test and Validation, ECE Dept., SIUC, May 2012. Currently with Intel Corporation, Santa Clara, CA. (Previously with Nvidia, CA, Qualcomm, CA, and Barefoot Networks, CA).
21. Manoj Kumar Goparaju, Coping with discrepancies of the manufactured weights in Threshold Logic gates, ECE Dept., SIUC, December 2009. Currently with Qualcomm, Raleigh, NC.
22. Michael N. Skoufis, Coping with delays and hazards in buses and random logic in deep sub-micron, ECE Dept., SIUC, August 2009. Currently with Sandia National Labs, NM. (Previously with Raytheon Inc., Tucson AZ).
23. Edward Flanigan, Scalable Test Generation for Path Delay Faults, ECE Dept., SIUC, January 2009. Currently with Northrop Grumman. (Previously with Boeing Corp., OK, and with Raytheon Inc., AZ).
24. Arkan Abdulrahman, Test Pattern Generation Techniques that target low Test Application Time, ECE Dept., SIUC, May 2008. Currently with Qualcomm Inc., San Diego, CA. (Previously with Marvell Inc., Phoenix, AZ).
25. Rajsekhar Adapa, Techniques for Improved Diagnosis, ECE Dept., SIUC, May 2008. Currently with Broadcom Inc. Previously with Qualcomm and Nvidia Inc, San Jose, CA.
26. Milir M. Vaseekar Kumar, ATPG and Fault Grading for Delay Faults, ECE Dept., SIUC, December 2006. Worked at Synopsys Inc., Mountain View, CA, after graduation. (Deceased.)
27. Khadija J. Stewart, Emerging technologies Involving Networks, ECE Dept., SIUC, August 2006. Currently a tenured Professor, Computer Science Dept., Depauw University, Newcastle, IN
28. Mohammad Moiz Khan, Re-synthesis for Intellectual Property Protection and Performance, ECE Dept., SIUC, August 2006. Currently with Synopsys Inc., Mountain View, CA.
29. Saravanan Padmanaban, Non-enumerative techniques for delay verification and diagnosis, College of Engineering, SIUC, August 2003. Currently with Intel Corporation, Hillsboro, OR. (Previously with the ECE Dept., Univ. of Maryland Baltimore County.)
30. Maria Michael, Test-based timing verification using functional techniques, College of Engineering, SIUC, 2002. Currently tenured Assoc. Professor, ECE Dept., Univ. of Cyprus. (Previously Assist. Professor, CSE Dept., Univ. of Notre Dame.)
31. Dimitrios Karayiannis, Delay Considerations in Testing and Synthesis of Integrated Circuits, College of Science, SIUC, August 1996. Currently President and COO at Korys Technologies. Previously VP of R&D at Inside Secure, France. Earlier with Texas Instruments Inc., CA, Synopsys Inc., CA, and Viewlogic Inc., CA.

co-advised

32. Cheng Luo (main advisor: W.-C. Hu), XML Selectivity Estimation, ECE Dept., SIUC, 2007. Currently with Computer Science Department, Coppin State University, Baltimore, MD
33. Zhewei Jiang (main advisor: W.-C. Hu), On XML query processing, ECE Dept., SIUC, 2007. Currently with the University of Maryland Baltimore County, Baltimore, MD.
34. Dimitri Kagaris (main advisor: F. Makedon), Pseudo-exhaustive built-in self-test, Computer Science Dept., Dartmouth College, 1994. Currently with the School of Electrical, Computer, and Biomedical Engr., SIUC.

Current supervision of Ph.D. students

- Vasileios Pentsos, Topic: Enhanced Deep Learning Neural Networks for Classification and Forecasting Problems in Embedded Systems.

- Chinthana Wimalasuriya. Topic: Adversarial Machine Learning in Neuromorphic Architectures.
- Danuka Malinda Lama Hewage. Topic: Point Cloud-based Image Reconstruction in Noisy Environments.

Supervised students with MS Theses (84 students)

- **ECE Dept., SIUC:** B. Lamichhane (2024), R. Ferdous (2024), K.I. Shafi (2023), O. Rijal (2022), S. Basaula (2022), A. Itani (2021), C. Sagili (2019), K. Samala (2018), D. Veskoukis (2018), F.M. Shakhiba (2018), E. Ahmadi (2016), A. Yadav (2016), T. Toulas (2015) V. Gkintzou (2014) B.S. Ali (2013), A. Watkins (2012), W. AlJubouri (2012), L. Pierce (2011), J. Lenox (2011), G. Panagiotakopoulos (2011), P. Alladi (2010), A.M. Somashekar (2010), A. Palaniswamy (2008), K. Karmakar (2008), R. Didla (2008), S.K. Gillela (2008), S. Gangadhar (2007), P. S. Ghandi (2007), D. Jayaraman (2006), J. Sheridan (2006), S. Dechu (2006), V.N. Koripalli (2006), E.L. Flanigan (2005), M.K. Goparaju (2005), C. Song (2005), L. Ghernoub (2004), S.N. Konidena (2004), J.N. Jayanna (2004), B. Soewito (2004), Y. Wang (2004), V.V.K. Akula (2004), M. Welling (2004), K.K. Vellakkat (2004), U. Kalyanasundaram (2004), M.M.V. Kumar (2004), T. Venkataraman (2004), S. Venkataramani (2004), Y. Devaraj (2003), S. Zhao (2003), A. Abdulrahman (2003), C. Kalapodas (2003), K. Kalaiselvam (2003). R. Rangunathann (2003), V. Nagarandal (2003), S. Kuriakose (2003), A. Mandadi (2003), G. Pani (2003), L. Pabbathi (2002), K. Ramanathan (2002), M. Khan (2002), M. Shah (2001), K. Stewart (2001), C. Proano (2001)
- **ECE Dept., U. of Arizona:** J. Deodhar (2000)
- **CS Dept., SIUC:** D. Demetriou (1998), A. Rodriguez (1998), M..K. Michael (1998), N. Denny (1998), R. Muezenberger (1998), W. Zhu (1998), J. Wang (1998), N. Zia (1996), C. Dinakaran (1996), N. Gaspar (1996), R. Koneru (1996), F.T. Al-Khamayseh (1995), E. Kofterou (1994), T. Walk (1993), E. Aleisa (1993), L. Mahmoodian (1993), J. Crenshaw (1993), D. Karayiannis (1993), M. Cubley (1993), T. Smith (1993)

Details on recently supervised MS theses (since 2014)

- Bishal Lamichhane, Multi-area Continuous-Time Optimal Power Flow and Generation Scheduling using a Distributed Algorithm, School of ECBE, November 2024.Currently with Electric Power Engineers (EPE), Austin, TX,
- ,Md. Rezoan Ferdous, Predicting YOLO Misdetection using Feature Map Activations. School of ECBE, SIUC, July 2023. Currently with the University of Florida (Ph.D. program in ECE).
- Md. Kamal Bin Shafi. Accelerated Cellular Traction Calculation by Predictions using Deep Learning, School of ECBE, SIUC, July 2023, Currently with North Carolina State University (Ph.D. program in ECE).
- Omkar Rijal, A Current-based Winner-Take-All (WTA) Circuit for Analog Neural Network Architecture, School of ECBE, SIUC, August 2022. Currently with Apple, Cupertino, CA.
- Sapan Basaula, Test Set Compaction Considering Test Application Time in Full Scan Circuits, School of ECBE, SIUC, June 2022. Currently with Synopsys, Mountain View, CA.
- Aashish Itani, Comparison of Adversarial Robustness of ANN and SNN towards Black Box Attacks, School of ECBE, SIUC, May 2021. Currently with Intel, Santa Clara, CA.
- Chandra Sagili, Multi-threading accelerator for SMT-based RTL verification, ECE Dept. SIUC, SIUC, October 2019. Currently with Cadence, CA.
- Keerthana Samala, Test Pattern Generation for Double Transition Faults, ECE Dept., SIUC, May 2018. Currently an embedded systems software engineer with Valeant Pharmaceuticals.
- Damianos Veskoukis, Automatic MC/DC Test Pattern Generation, ECE Dept., SIUC, June 2018. Currently with Infineon Technologies, Munich, GR.
- Fatemeh Mohammadi Shakiba, CMOS-based implementation of hyperbolic tangent activation function for artificial neural network, ECE Dept., SIUC, March 2018. Currently with NJIT (PhD program).
- Ajitkumar Yadav, Fault Diagnosis in Failed Functional Sequences at RTL Level, ECE Dept., SIUC, August 2016. Currently with AMD, Orlando, FL.
- Ehsan Ahmadi, Solving Incremental Specifications using Z3 SMT Solver, ECE Dept., SIUC, (August 2016). Currently with the Univ. of Wisconsin (PhD program).
- Theodore Toulas, Transition fault-driven delay defect diagnosis in the presence of process variations, ECE Dept., SIUC, December 2015. Currently with Synopsys, Mountain View, CA.
- Vasiliki Gkintzou, Preemptive edge-based scheduling for Real-time Networks On-a-Chip, ECE Dept., SIUC, October 2014. Currently with Advantest, San Jose, CA.

Current supervision of MS students with thesis option

- Sunimal Rathanayake: Recurrent and Convolutional Neural Network-based Methods in Molecular Mechanics.
- Krishna Dahal: AI-assisted Circuit Health Monitoring.
- Iresh Jayawaradana. Topic: IC Delay Testing using Deep Learning.
- Sabita Khadha. Topic: T.B.A.